Voltage Islanding Technique for Concurrent Power and Temperature Optimization in 3D-stacked ICs

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***Abstract*— Voltage island (VI) is a set of well-known techniques aimed at achieving power reduction. However, most previous VI methods are not capable of directly controlling the peak temperature even though high peak temperature is an important cause of reliability problems. This uncontrollability is more critical in three-dimensional (3D) die-stacked ICs due to the much higher power density (and therefore higher temperature) than in the 2D case. To solve this issue, we propose a heuristic VI method for 3D-stacked ICs, which simultaneously optimizes power consumption and peak temperature. Another highlight of our method is that overhead of VI is accurately controlled by the number of voltage islands unlike previous VI methods relying on inaccurate fragmentation cost.**

Keywords—3D-stacked IC, low power design, thermal-aware, multiple supply voltage, voltage island

I. INTRODUCTION

Voltage island (VI) is an effective technique which provides power reduction for an IC by dividing the power domain of an IC into several islands powered by the different voltage source [1]. Since blocks in an IC may have different performance requirements, different clock frequencies and voltages can be used rather than supplying a single voltage decided by the fastest operating block. By using multiple supply voltages, unnecessary power caused by oversupplied voltages can be avoided. Also, VI can be an attractive thermal management method because the reduction in power density leads to the reduction in heat density.

There have been many VI methods in 2D domain focusing on power reduction. Even though most VI methods reduce the temperature as a by-product of power reduction, power-only optimization may not reduce the peak temperature in the worst case. Compared with 2D methods, there have been only few works for VI in 3D domains although both power and temperature issues become more critical in 3D ICs [2].

Whereas VI is an effective method to reduce power and temperature, the number of possible voltage islands is limited because increasing the number of power domains causes non-marginal overheads. Increasing the number of power domains not only requires additional power network resources but also complicates other steps of design flow such as floorplanning and timing analysis [3]. Because of these overheads, the number of allowed voltage islands should be limited. However, many of previous VI works are not capable of accurately controlling the number of voltage islands while relying on fragmentation cost which leads to poor control over the number of voltage islands [4].

To overcome the limitation of the existing works, we propose a novel 3D VI method which minimizes both peak temperature and power consumption concurrently while precisely controlling the number of voltage islands.

II. 3D VI PROBLEM FORMULATION

Before the detailed description of our 3D VI technique, we define a problem to be solved via VI.

Inputs:

· The set of tiers *K*, where $k \in K$ ($1 \le k \le |K|$) denotes a tier of the given 3D IC.

· The set of blocks *B*, where $blk_i^k \in B^k$ ($1 \le k \le K$, $1 \le i \le |B^k|$) denotes a block at tier number *k*. The dimension, the minimum required voltage level, and the power density at the reference voltage level of each blk_i^k are also given.

· The floorplan of a 3D IC and the adjacency graphs of the blocks for all tiers (an adjacency graph per a tier), which show the connectivity between blocks.

· The set of available voltage levels *V*, where $v_p \in V$ ($1 \le p \le |V|$) denotes a voltage level.

· The maximally allowed number of voltage islands is *N*.

Problem Definition: Given these inputs, the proposed 3D VI method assigns a voltage level $v_p \in V$ to each block $blk_i^k \in B^k$ such that total cost defined in Eqn. 1 is minimized under the constraint of the maximally allowed number of voltage islands.

$$cost = w_P \cdot P_{total} + (1 - w_P) \cdot T_{peak} \quad (1)$$

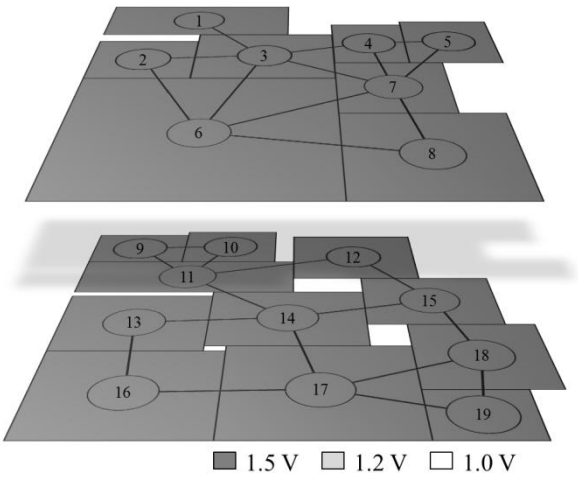
where P_{total} and T_{peak} are power consumption and peak temperature respectively, and w_P is a user-defined weighting coefficient.

The overhead introduced by the VI technique is controlled by constraining the number of voltage islands, *N*. We do not consider area and power overheads incurred by level shifters because they are negligible compared with those of the blocks. Specifically, a low-to-high level shifter is composed of 10 transistors (3 inverters and a differential amplifier), and a high-

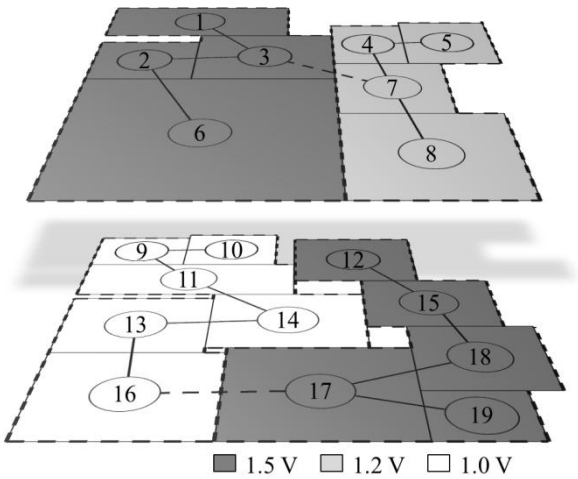
to-low level shifter is of just 4 transistors (2 inverters) [3]. By neglecting the level shifter overheads, the complexity of our 3D VI method can be greatly reduced at a marginal sacrifice in terms of accuracy. We also assume that registers exist at the input and output ports of each block, and thus there is no need to consider the critical timing path between any two blocks in our work.

III. PROPOSED 3D VI METHOD

We first introduce the data structure called a *neighbor-tree* which plays a crucial role in our 3D VI method for the accurate control of the number of voltage islands. The neighbor-tree is generated for each tier from input the adjacency graphs, where a vertex represents a block and an edge between two vertices represents the adjacency of the corresponding blocks. Also, it can be partitioned into subtrees. Each subtree represents a group of neighboring blocks sharing the same power supply voltage, which is referred as a voltage island. Therefore, partitioning a neighbor-tree creates voltage islands and the number of voltage islands can be controlled easily.



(a) Adjacent graphs for a given 3D floorplan with a single 1.5V supply voltage



(b) Partitioned neighbor-trees for the floorplan after 3D VI

Fig. 1: Illustration of the proposed 3D VI method

To explain the overall method, we introduce an example of a 2-tier 3D IC (Fig. 1). Taking the adjacency graphs in Fig. 1a (extracted from 3D floorplan) as inputs, our 3D VI method assigns the blocks of all tiers to voltage islands, concurrently reducing vertical heat flow as well as power consumption. Our 3D VI takes a heuristic approach which transforms an adjacency graph for each tier into a neighbor-tree and optimally partitions all neighbor-trees simultaneously into appropriate voltage islands to optimize vertical heat flow and power consumption as shown in Fig. 1b.

Algorithm 1 shows the top-level procedure of the proposed 3D VI method. The main goal of this heuristic 3D VI method is to explore the local solution space around a given starting point (initial neighbor-trees) in a greedy manner by iteratively performing a modify-and-evaluate operation of the neighbor-trees.

Algorithm 1 Heuristic 3D VI

1: generate initial neighbor-trees for all tiers
2: **for** $1 \le k \le |K|$
3: **for** $blk_i^k \in B^k$ **do**
4: $e_{victim} \leftarrow$ edge between blk_i^k and its parent
5: $E^{replace} \leftarrow$ {edges which are candidates to replace e_{victim}}
6: **for** $e \in E^{replace}$ **do**
7: reconnect e in neighbor-tree and cut the originally connected edge, e_{victim}
8: *3D-aware neighbor-tree partitioning*
9: update the best solution

We first generate initial neighbor-trees for each tier by pruning less important edges in the adjacency graphs (line 1 of Algorithm 1). Then, we visit each vertex, blk_i^k, and iteratively generate the variants of the initial neighbor-tree in tier *k*. For blk_i^k, we generate a variant of the neighbor-tree by replacing e_{victim} with an edge in $E^{replace}$ (line 7). Next, we partition the neighbor-trees for all tiers with the variant for tier *k* considering the peak temperature (concurrently for all tiers) via MILP (Mixed Integer Linear Programming), which returns the optimum solution for the partitioning (line 8). To calculate the peak temperature during the partitioning, we employ the resistive thermal model in [5]. If the solution is better than the best solution obtained so far, we update the best solution and keep the current variant. Otherwise, the current variant is discarded and the previous one is kept. The step for the variant generation and evaluation (from line 6 to line 9) is iteratively performed until no more possible variant can be found for all vertices.

IV. EXPERIMENTS

A. Experimental Settings

We use ami49 (49 blocks) from MCNC benchmarks, n50 (50 blocks) from GSRC benchmarks, and our synthetic benchmark, rg50 (50 blocks) for validation. We assume four tiers for the 3D implementation of each benchmark. We use a thermal-aware 3D floorplanner [6] to generate floorplans of benchmarks. In order to assign appropriate power value to each block, we adopt the way used in [5]. Each block has its own minimum legal voltage level to satisfy the given performance and/or power constraints. We also assume five feasible voltage levels: $0.9V$, $1.0V$, $1.2V$, $1.3V$, and $1.5V$. The number of voltage islands allowed is set to 12, i.e., 3 per tier. We implement our method in C++ and solve the MILP formulation by Xpress-MP [7]. We conduct all experiments on a 2.13GHz Intel Core2duo CPU with 3GB memory.

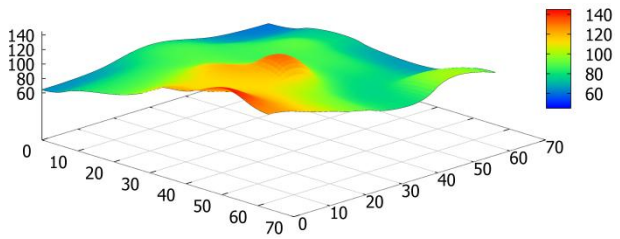
B. Experimental results

Table 1 shows the experiment results for the proposed 3D VI method when it optimizes only power consumption (w_P = 1) or both power consumption and peak temperature (w_P = 0.5). On average, thermal-unaware 3D VI (w_P = 1) reduces the peak temperature by 2.39 % and the power consumption by 23.39 % compared with the design supplied by a single voltage. When we consider power as well as vertical heat flow (w_P = 0.5), the peak temperature is reduced by 22.08 % on average while power dissipation is slightly increased by 1.35 % on average compared with the case of no temperature consideration (w_P = 1) due to temperature consideration.

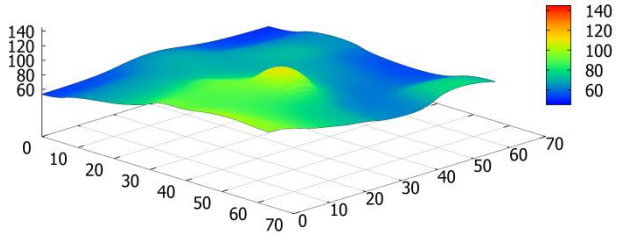
Table 1: Comparison between thermal-unaware VI and thermal-aware 3D VI (Note that % denotes reduction from the design without VI)

	thermal-unaware VI (w_P = 1)			thermal-aware VI (w_P = 0.5)		
test bench	P_{total} %	T_{peak} %	runtime sec	P_{total} %	T_{peak} %	runtime sec
ami49	22.77	2.75	10.03	22.13	8.53	11.38
n50	17.35	0	7.72	16.12	13.84	9.08
rg50	30.06	4.42	15.12	27.87	51.03	22.12
avg.	23.39	2.39	10.96	22.04	24.47	14.19

Fig. 2 shows the temperature maps of the top tiers obtained from applying two methods (no VI and thermal-aware VI) for rg50. In temperature maps, the *xy*-plane denotes the horizontal physical locations of a tier and the z-axis shows temperature values obtained from Hotspot [8] for corresponding locations. We show top tiers because the top tier is farthest from the heat sink and the hottest tier. The one without VI, Fig. 2a, show prominently higher temperature than the other one. Fig. 2b shows the result from the proposed thermal-aware 3D VI method. We can observe that the peak temperature is reduced further compared with the one without VI because the hottest regions are eliminated by preventing vertically adjacent blocks from being assigned to high voltage levels.



(a) without voltage islanding



(b) after thermal-aware VI ($w_P = 0.5$)

Fig. 2: Temperature map of the topmost tier in rg50

V. CONCLUSION

We have proposed a novel VI method for 3D-stacked systems which optimizes both power consumption and peak temperature simultaneously under the constraint of the number of voltage islands. The experimental results strongly support the need for temperature considerations when using VI for temperature-critical 3D ICs.

ACKNOWLEDGMENT

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